

NCP3284A 40 A Reference Design

TND6524/D

Description

The NCP3284A reference design demonstrates the NCP3284A single-phase synchronous buck regulator with integrated power MOSFETs and a 49.5 A valley current limit. The design was tested with an input voltage of 8 V to 16 V and can deliver up to 40 A output current. The device uses a current mode, constant-on-time architecture with enhanced ramp pulse modulation (eRPM) to provide an ultra-fast transient response while using minimal output capacitance. The integrated 1.1 mΩ/3 mΩ power switches ensure high efficiency and minimal power dissipation for high output currents. This reference design demonstrates two operating points (VOUT = 1 V and 3.3 V) with both a low profile design (all components < 3.1 mm) and a higher efficiency design with a larger (less lossy) inductor.

NCP3284A Features

- 4.5 V to 18 V Input Voltage Range
- Resistor programmable 500 kHz/600 kHz/800 kHz/1 MHz switching frequency (MODE/FSET)
- External FB input with remote voltage sense (FB, VSNS-)
- Optional fixed frequency FCCM or auto DCM (MODE/FSET)
- Integrated 5 V LDO for gate drive with an external supply option (VDRV)
- Enable input with resistor programmable hysteresis (EN)
- Resistor programmable soft-start (SS)
- Resistor programmable valley current limit (ILIM)
- Thermal shutdown protection (150 °C)
- Selectable fault shutdown or auto restart (HICCUP)
- Open Drain Power Good Indicator (PGOOD)

Typical Application Circuit

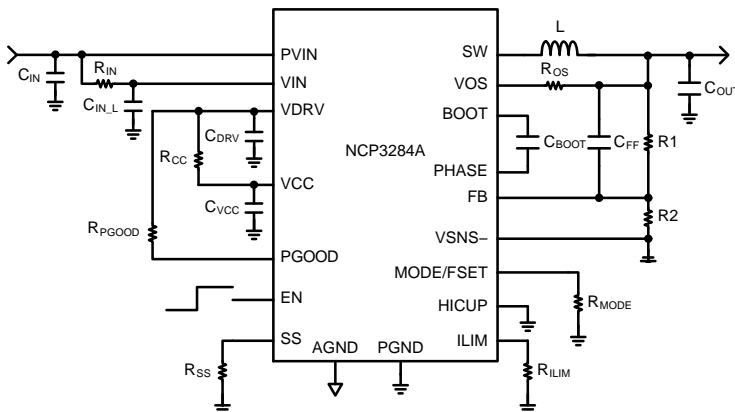


Figure 2. Typical Application Circuit

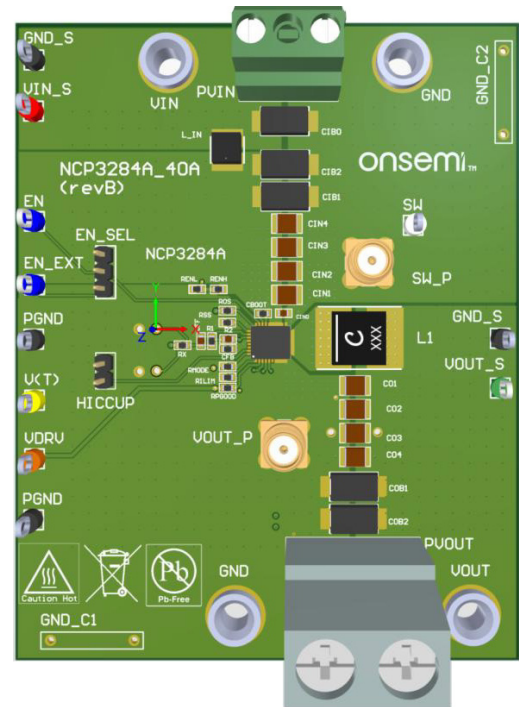


Figure 1. Board Photo

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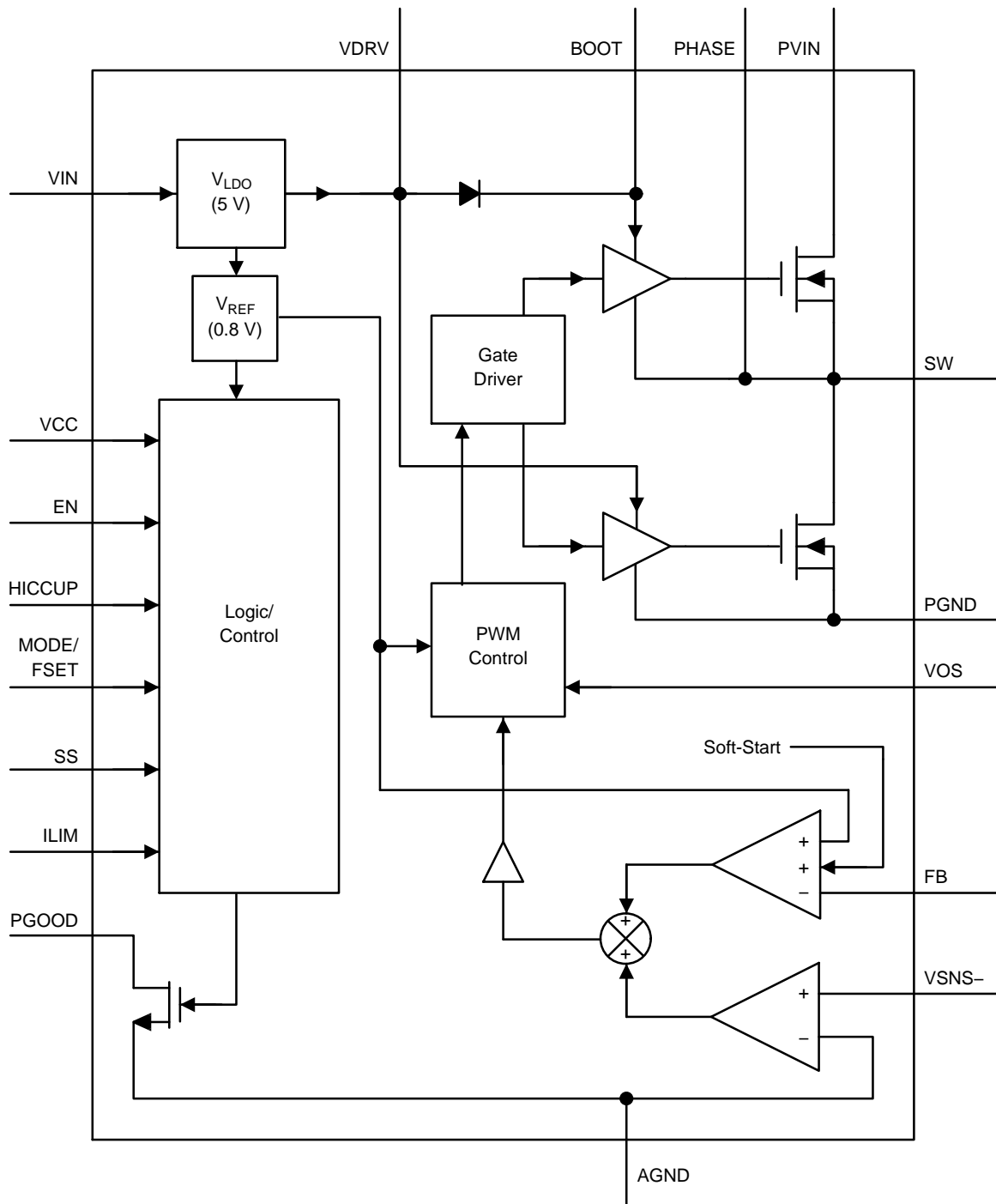


Figure 3. Simplified Block Diagram

DEVICE OVERVIEW

The NCP3284A is an adaptive constant on time buck converter which operates in PFM operation at light and medium loads and transitions into a pseudo fixed frequency PWM mode at heavy loads. The device can source up to 40 A output current and operates from a 4.5 V to 18 V input voltage. Resistor programmable switching frequency options include (500 kHz, 600 kHz, 800 kHz, and 1 MHz).

This reference design showcases two operating points: a 3.3 V output and a 1 V output with a switching frequency of 1 MHz.

Input Filter

The input filter consists of a 100 μ F capacitor (CIB0) and a 130 nH inductor (L_IN). This filters the switching ripple at the NCP3284A's input and shields the supply from excessive noise.

Output Capacitance (COUT)

The output capacitance array is composed of 4x 47 μ F ceramic capacitors and 2x 330 μ F bulk capacitors. This keeps the switching ripple at the output very low and helps reduce the output voltage overshoot during a load release.

OUTPUT OVP DETECTION

The NCP3284A features an over voltage protection (OVP) which is engaged when the feedback node exceeds 1 V (typ), 0.95 V min (for >1 μ s). This equates to a 20% nominal increase in VOUT before OVP is triggered. Once triggered the NCP3284A will turn off and go through a hiccup timeout before a re-start is attempted. Very fast slew rates during load release can cause an output voltage overshoot and cause VOUT to exceed the VOVP threshold. If this is an issue, more bulk output capacitance might be required, or a slower IOUT slew rate during a load release.

Enable Input

The reference design includes a three pin EN_SEL header which can be jumpered for a VIN controlled enable or jumpered for a direct access to EN via the EN_EXT clip. When EN_SEL is jumpered between middle and top pins, the on board resistive divider from VIN to EN (RENH = 95.3 k Ω and RENL = 27.4 k Ω) divides VIN and forces the device to turn on when VIN rises above 6.92 V. The hysteresis will then force the device to turn off when VIN falls below 5.46 V.

When EN_SEL is jumpered between the middle and bottom pins EN can be driven directly from EN_EXT. When this is the case the device will turn on when EN_EXT is driven above 1.43 V and will turn off when EN_EXT is driven below 1.22 V.

Inductor

Two inductors are used for this reference design. For a low profile solution (<3.1 mm total) the inductor is an XGL7030-241 from Coilcraft. Nominal inductance is 0.24 μ H with a 46 A maximum current at 30% reduction from nominal inductance. Typical DC resistance is 1.1 m Ω . An

alternate inductor (the FP1108-R21-R) from Eaton, offers a lower DC resistance of 0.20 m Ω , but a higher case height of 7.5 mm. The difference in efficiency is shown in (Figure 8 vs. Figure 9) and (Figure 21 vs. Figure 22).

VDRV

VDRV is the output of the internal 5 V LDO. VDRV is powered from VIN and provides the gate drive for the power FETs as well as the internal bias VCC. VDRV is connected to VCC through an external RC filter.

External VDRV

An optional configuration with an external VDRV is possible which can slightly increase efficiency. For this configuration, PVIN would be driven from 12 V while VIN, VDRV, and VCC would be connected to an external 5 V supply. Plots showing the boost in efficiency with an external 5 V drive voltage are shown in the typical characteristic curves (see Figure 10/11 and 23/24).

The following figures show the current requirement into IN, VCC, and VDRV when driven from an external 5 V.

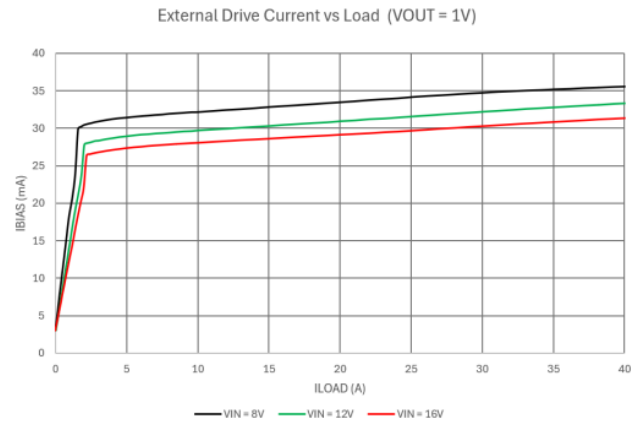


Figure 4. External Drive Current (VOUT = 1 V)

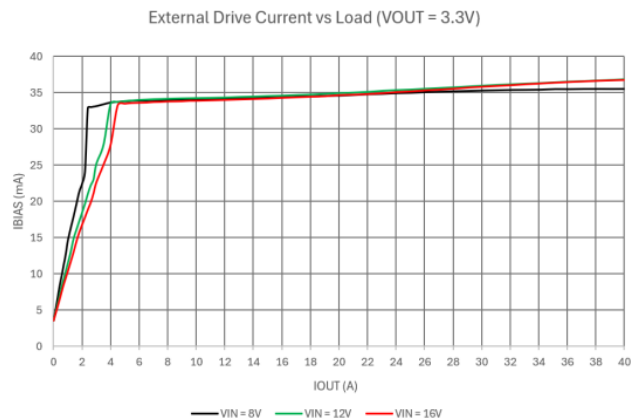


Figure 5. External Drive Current (VOUT = 3.3 V)

Thermistor

The reference design includes a bottom side NTC thermistor which reports the board temperature as a voltage proportional to temperature at the V(T) test point. The

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thermistor is a 470 kΩ negative temperature coefficient (NTC) with a beta ($\beta = 4306K$). A parallel resistor ($R_P = 40\text{ k}\Omega$) is used to linearize the NTC's response around the 25 °C to 150 °C temperature range. The circuit is biased from VDRV with a low side 10 kΩ resistor. Typical V(T) vs. temperature is shown below. There is an approximate 30 °C gradient from the thermistor divider temperature to the

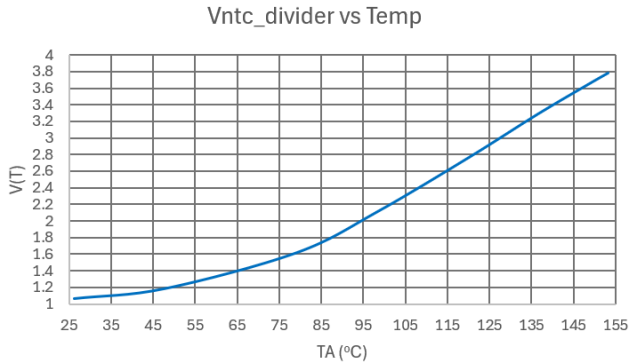


Figure 6. V(T) Voltage vs. Temperature

Using the thermistor's typical response, the steady state board temperature is shown for both configurations below.

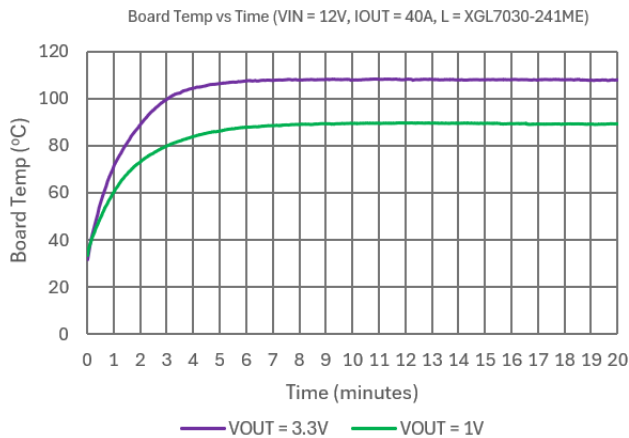


Figure 7. Board Temperature vs. Time (TA = 25 °C, Still Air)

MODE/FSET

MODE/FSET is configured with a RMODE = 40 kΩ which programs the device for DCM operation with a PWM frequency of 1 MHz.

Valley Current Limit

The NCP3284A senses over current using the low side (valley current). The options are:

Table 1.

R _{LIM}	I _{VALLEY}
33.2 kΩ	49.5 A
30.1 kΩ	45.5 A
24.9 kΩ	37.5 A
21.5 kΩ	32.5 A
16.2 kΩ	24.5 A
12.1 kΩ	18 A

The reference design is set with R_{LIM} = 33.2 kΩ.

Power Good

Power Good (PGOOD) is an open drain indicator which goes high Z when soft-start ends. The board has PGOOD pulled up to VDRV.

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Table 2. NCP3284A PERFORMANCE CHARACTERISTICS SUMMARY (3.3 V DESIGN)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VIN	Input Voltage Range		8	12	16	V
VOUT	Output Voltage			3.3		V
IOUT	Output Current Range		0		40	A
fsw	Switching Frequency	IOUT = 40 A		1		MHz
	Efficiency	IOUT = 40 A, PVIN = VIN = 12 V	L = XGL7030-241ME	91.7		%
			L = FP1108R1-R21-R	93.4		
Tboard	Board Temperature	15 min. soak time, IOUT = 40 A, TA = 25 °C, no forced air, L = XGL7030-241ME		108		°C
ΔVout	Output Voltage Undershoot During Load Step	IOUT from 0.1 A to 40 A		31		mV
	Output Voltage Overshoot During Load Release	IOUT from 40 A to 0.1 A		58		mV
VLOAD(12V)	Load Regulation	VIN = 12 V, IOUT from 0 to 40 A		0.33		mV/A
VLINE(40A)	Line Regulation	IOUT = 40 A, VIN from 8 V to 16 V		0.27		mV/V
VLINE(0)		IOUT = 0, VIN from 8 V to 16 V		0.52		mV/V
VRIPPLE	Output Voltage Ripple	IOUT = 40 A, BW = 20 MHz		22.4		mVpp
tSTART	Start-up Time	EN low to high to VOUT = 95% target, SS = 0		1.9		ms
fc	Crossover Frequency	IOUT = 40 A, L = XGL7030-241ME		460		kHz
Phase	Phase Margin	IOUT = 40 A, L = XGL7030-241ME		53		degrees

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TYPICAL CURVES (VOUT = 3.3 V)

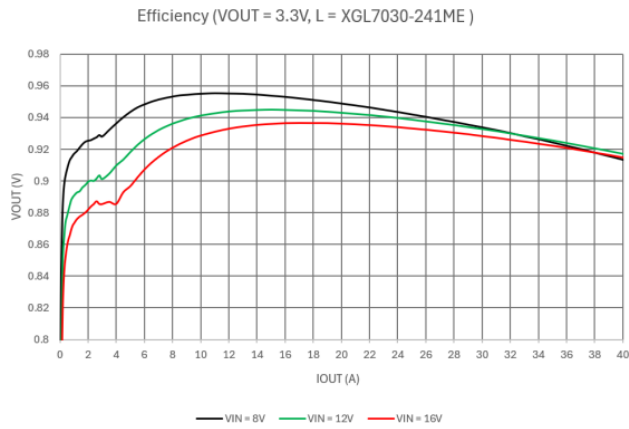


Figure 8. Efficiency vs. Load (Internal LDO)
(PVIN = VIN = 12 V)

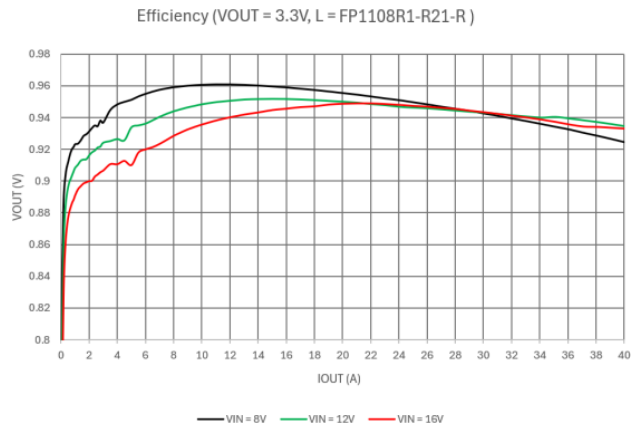


Figure 9. Efficiency vs. Load (Internal LDO)
(PVIN = VIN = 12 V)

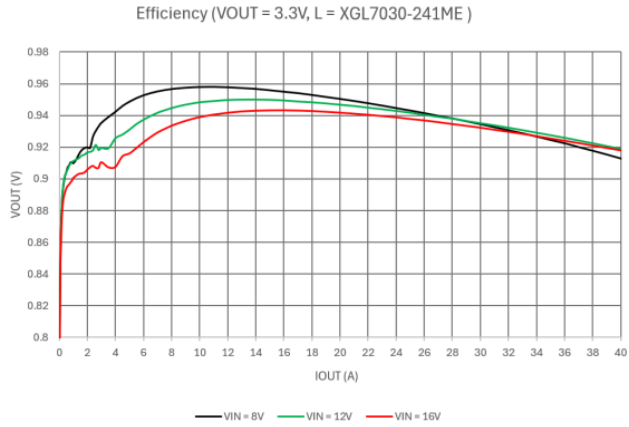


Figure 10. Efficiency vs. Load (External LDO)
(PVIN = 12 V, VIN = VDRV = VCC = 5 V)

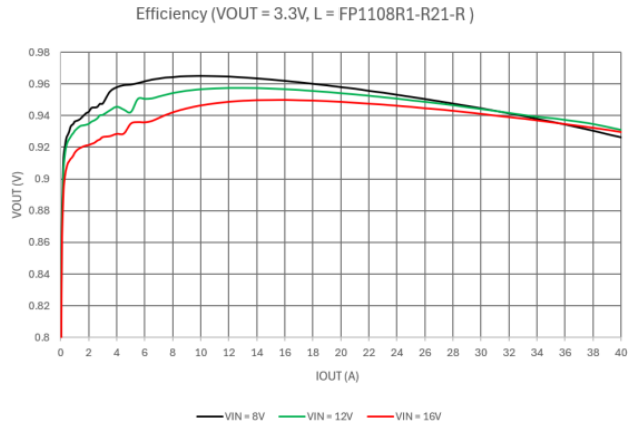


Figure 11. Efficiency vs. Load (External LDO)
(PVIN = 12 V, VIN = VDRV = VCC = 5 V)

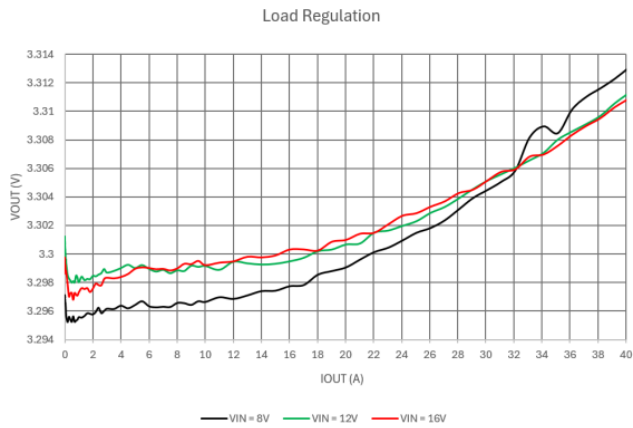


Figure 12. Load Regulation (VOUT = 3.3 V, IOUT = 40 A)

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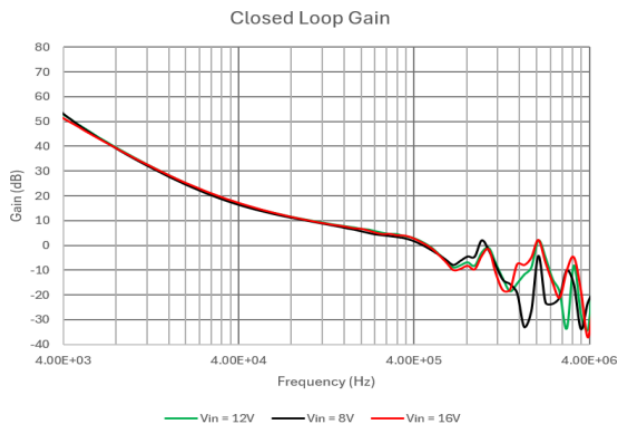


Figure 13. Closed Loop Gain (IOUT = 40 A)



Figure 14. Closed Loop Phase (IOUT = 40 A)

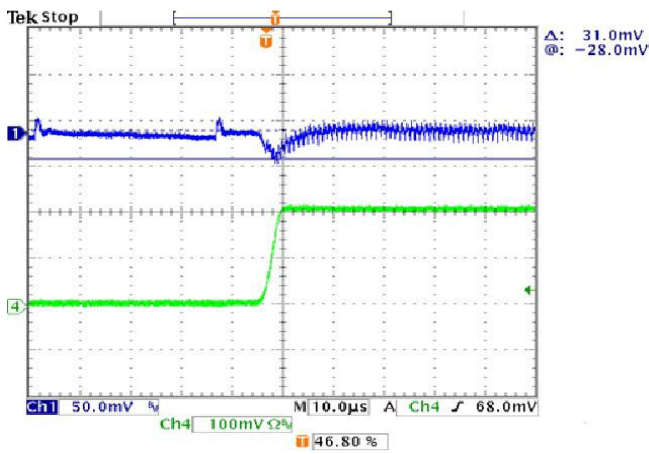


Figure 15. Load Step (0.1 A to 40 A), 10 A/μs
Ch1 = VOUT, Ch4 = IOUT (5 mV/A)

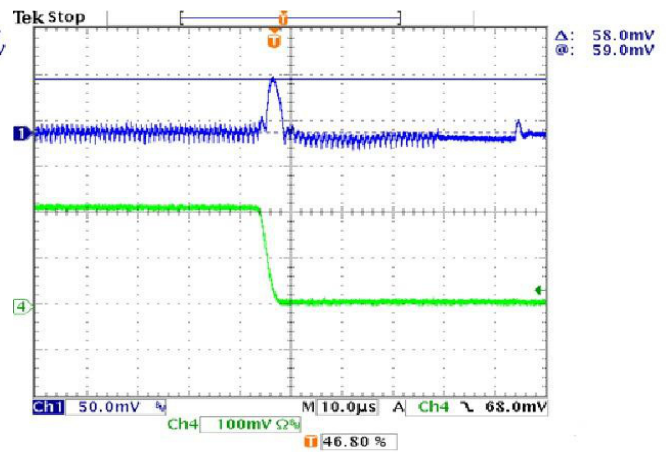


Figure 16. Load Release (40 A to 0.1 A), -10 A/μs
Ch1 = VOUT, Ch4 = IOUT (5 mV/A)

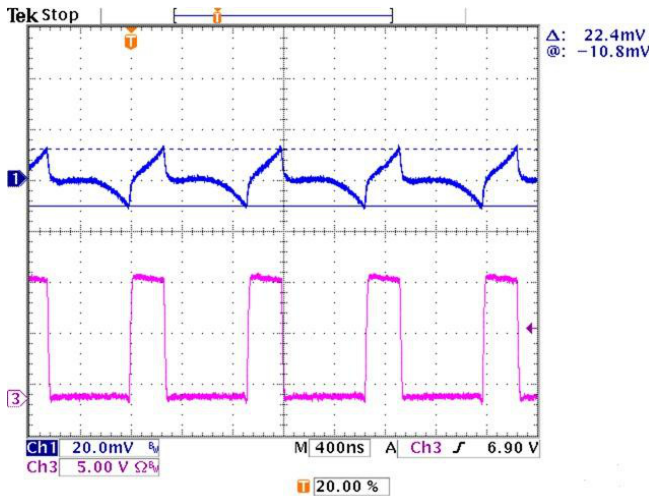


Figure 17. Output Voltage Ripple (IOUT = 40 A)
Ch1 = VOUT, Ch3 = VSW, BW = 20 MHz

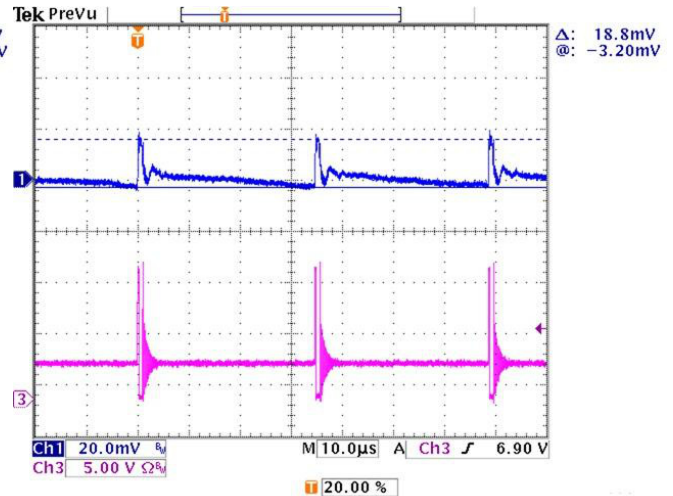


Figure 18. Output Voltage Ripple (IOUT = 100 mA)
Ch1 = VOUT, Ch3 = VSW, BW = 20 MHz

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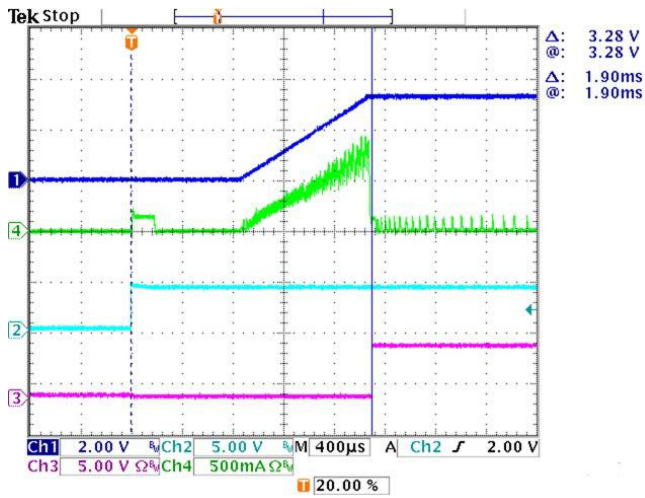


Figure 19. Start-Up (No Load)
Ch1 = VOUT, Ch4 = IIN, Ch2 = EN, Ch3 = PGOOD

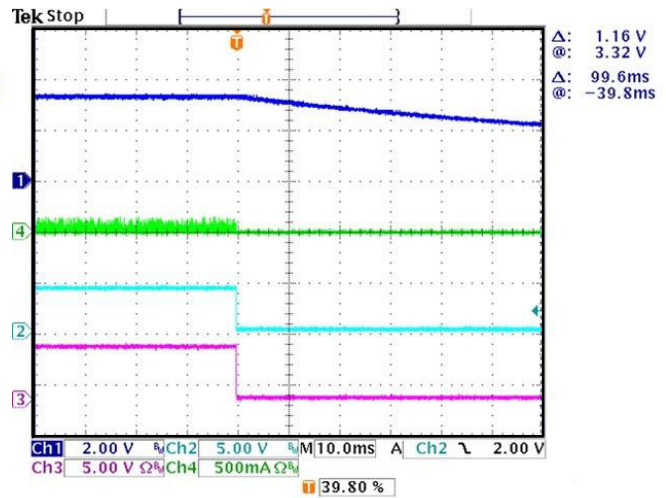


Figure 20. Shutdown (200 Ω Load)
Ch1 = VOUT, Ch4 = IIN, Ch2 = EN, Ch3 = PGOOD

Table 3. NCP3284A PERFORMANCE CHARACTERISTICS SUMMARY (1 V DESIGN)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VIN	Input Voltage Range		8	12	16	V
VOUT	Output Voltage			1		V
IOUT	Output Current Range		0		40	A
fsw	Switching Frequency	IOUT = 40 A		1		MHz
	Efficiency	IOUT = 40 A, PVIN = VIN = 12 V		80.8		%
		L = XGL7030-241ME L = FP1108R1-R21-R		83.6		
Tboard	Board Temperature	15 min. soak time, IOUT = 40 A, TA = 25 °C, no forced air, L = XGL7030-241ME		88		°C
ΔVout	Output Voltage Undershoot During Load Step	IOUT from 0.1 A to 40 A		37		mV
	Output Voltage Overshoot During Load Release	IOUT from 40 A to 0.1 A		79		mV
VLOAD(12V)	Load Regulation	VIN = 12 V, IOUT from 0 to 40 A		0.056		mV/A
VLINE(40A)	Line Regulation	IOUT = 40 A, VIN from 8 V to 16 V		0.032		mV/V
VLINE(0)		IOUT = 0, VIN from 8 V to 16 V		0.093		mV/V
VRIPPLE	Output Voltage Ripple	IOUT = 40 A, BW = 20 MHz		14		mVpp
tSTART	Start-up Time	EN low to high to VOUT = 95% target, SS = PGND		1.91		ms
Fc	Crossover Frequency	IOUT = 40 V, L = XGL7030-241ME		430		kHz
Phase	Phase Margin	IOUT = 40 V, L = XGL7030-241ME		85		degrees

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TYPICAL CURVES (VOUT = 1 V)



Figure 21. Efficiency vs. Load (Internal LDO)
(PVIN = VIN = 12 V)

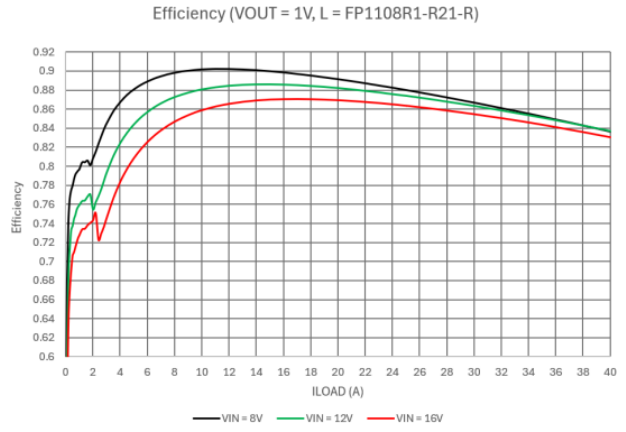


Figure 22. Efficiency vs. Load (Internal LDO)
(PVIN = VIN = 12 V)

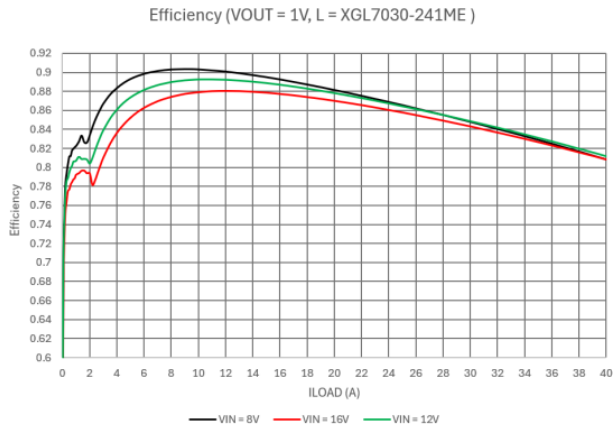


Figure 23. Efficiency vs. Load (External LDO)
(PVIN = 12 V, VIN = VDRV = VCC = 5 V)

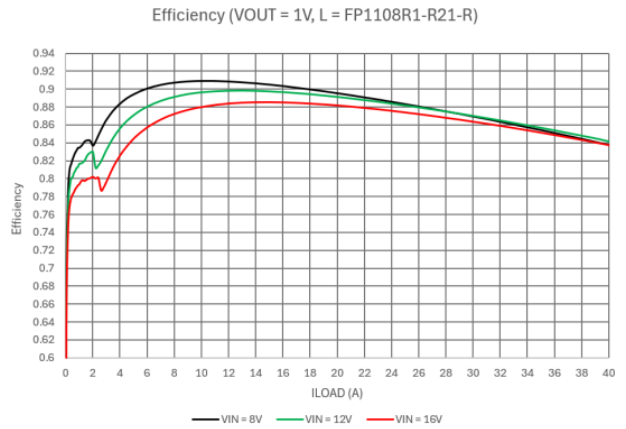


Figure 24. Efficiency vs. Load (External LDO)
(PVIN = 12 V, VIN = VDRV = VCC = 5 V)

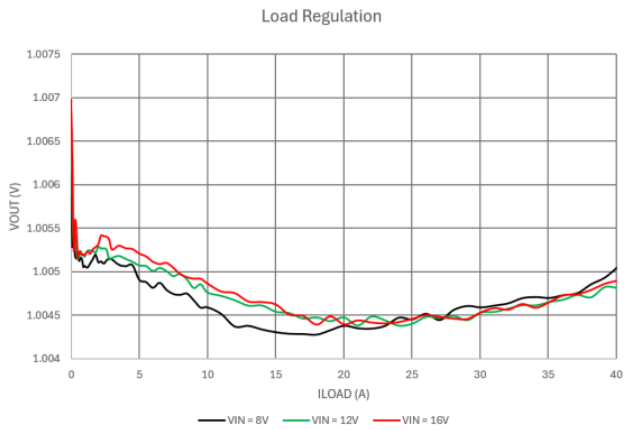


Figure 25. Load Regulation (VOUT = 3.3 V, IOU = 40 A)

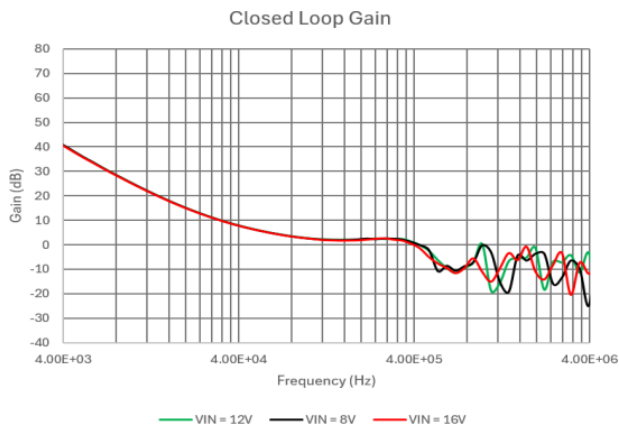


Figure 26. Closed Loop Gain (IOUT = 40 A)

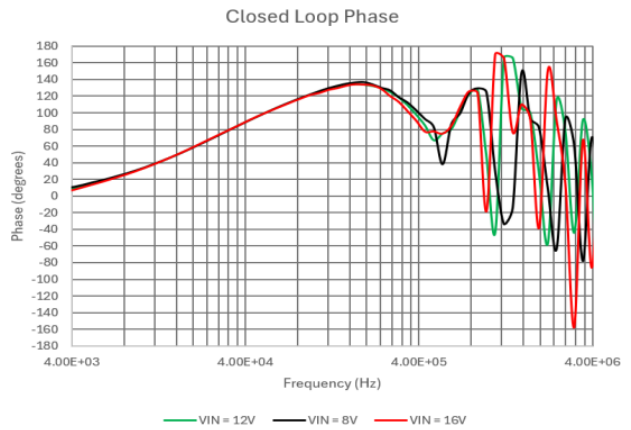


Figure 27. Closed Loop Phase (IOUT = 40 A)

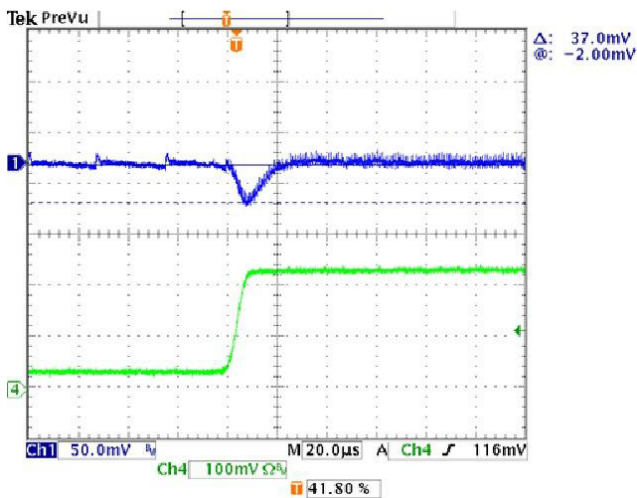


Figure 28. Load Step (0.1 A to 40 A), 5 A/μs
Ch1 = VOUT, Ch4 = IOUT (5 mV/A)

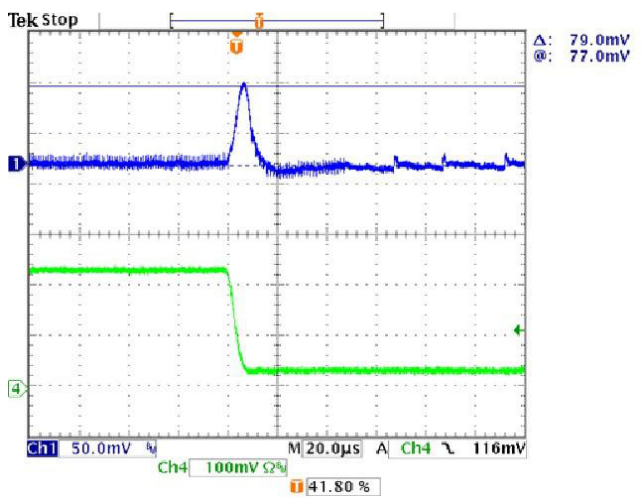


Figure 29. Load Release (40 A to 0.1 A), -5 A/μs
Ch1 = VOUT, Ch4 = IOUT (5 mV/A)

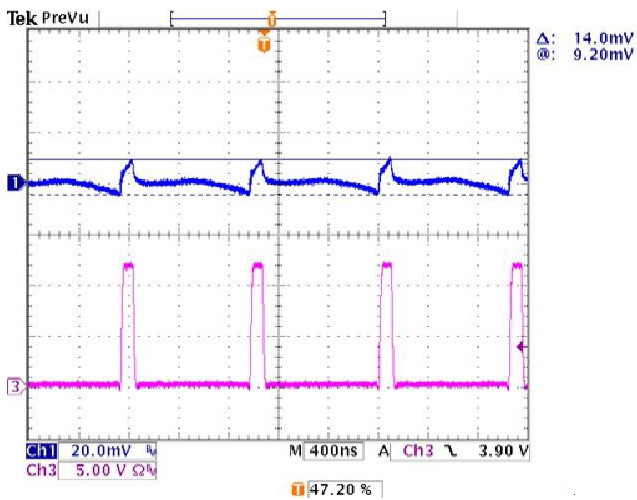


Figure 30. Output Voltage Ripple (IOUT = 40 A)
Ch1 = VOUT, Ch3 = VSW, BW = 20 MHz

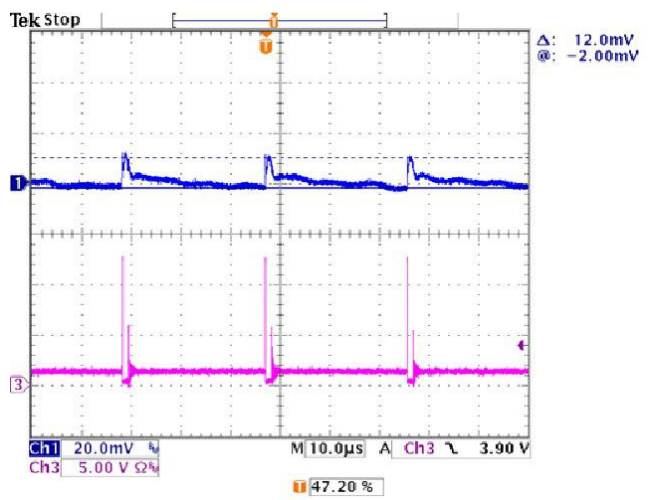


Figure 31. Output Voltage Ripple (IOUT = 100 mA)
Ch1 = VOUT, Ch3 = VSW, BW = 20 MHz

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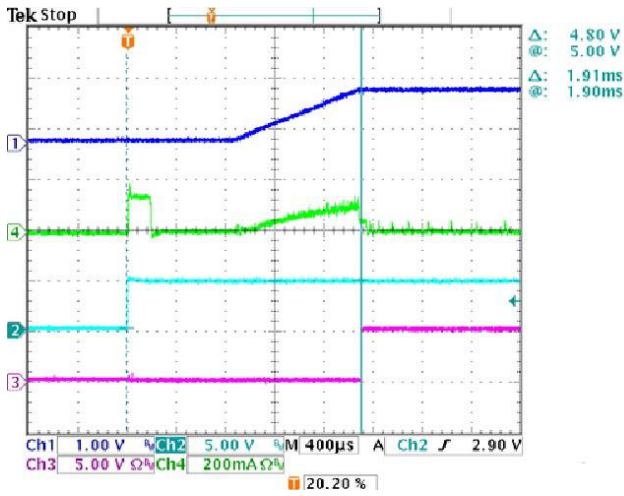


Figure 32. Start-Up (No Load)
Ch1 = VOUT, Ch4 = IIN, Ch2 = EN, Ch3 = PGOOD

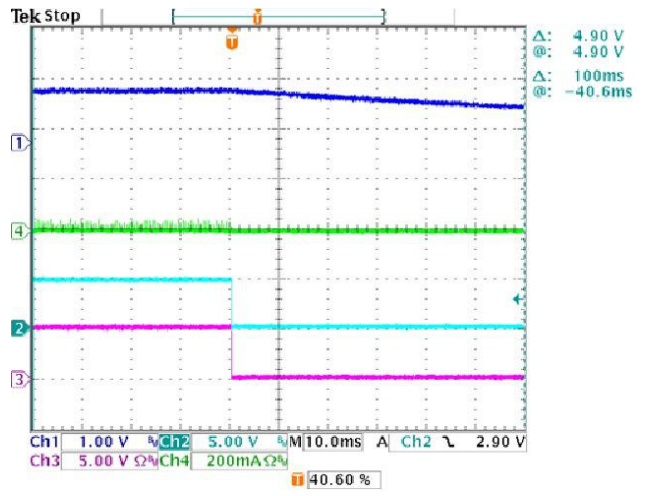


Figure 33. Shutdown (200 Ω Load)
Ch1 = VOUT, Ch4 = IIN, Ch2 = EN, Ch3 = PGOOD

SCHEMATIC

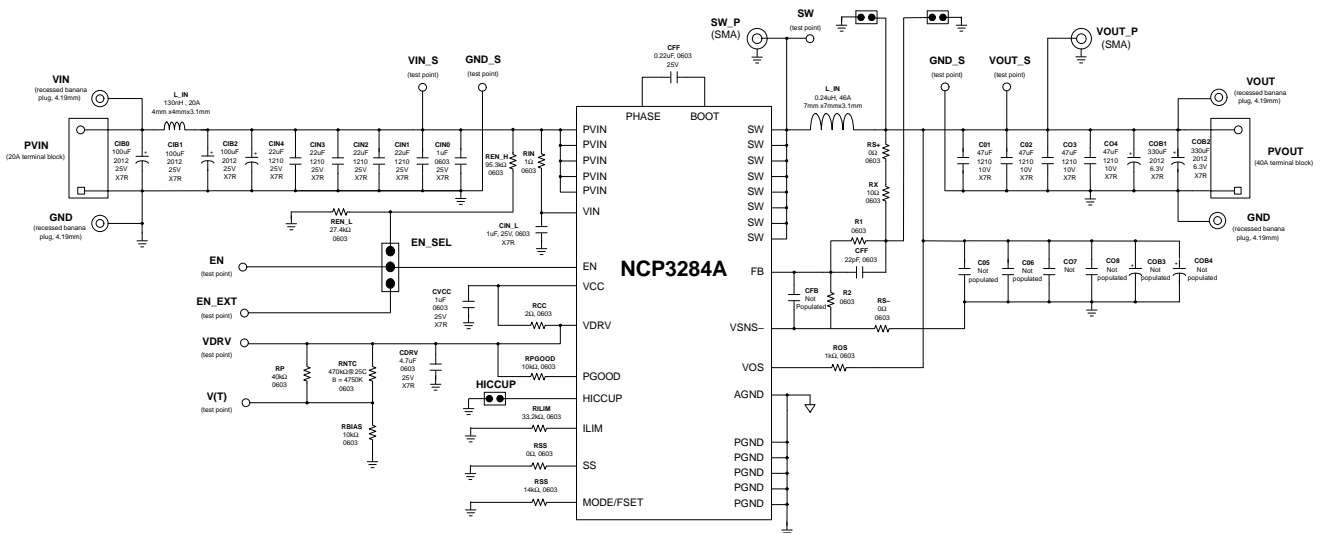


Figure 34. Schematic

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PCB LAYOUT

The reference design has 6 layers with 2 oz copper per layer. Total board thickness is 41 mil. The following figures show each layer.

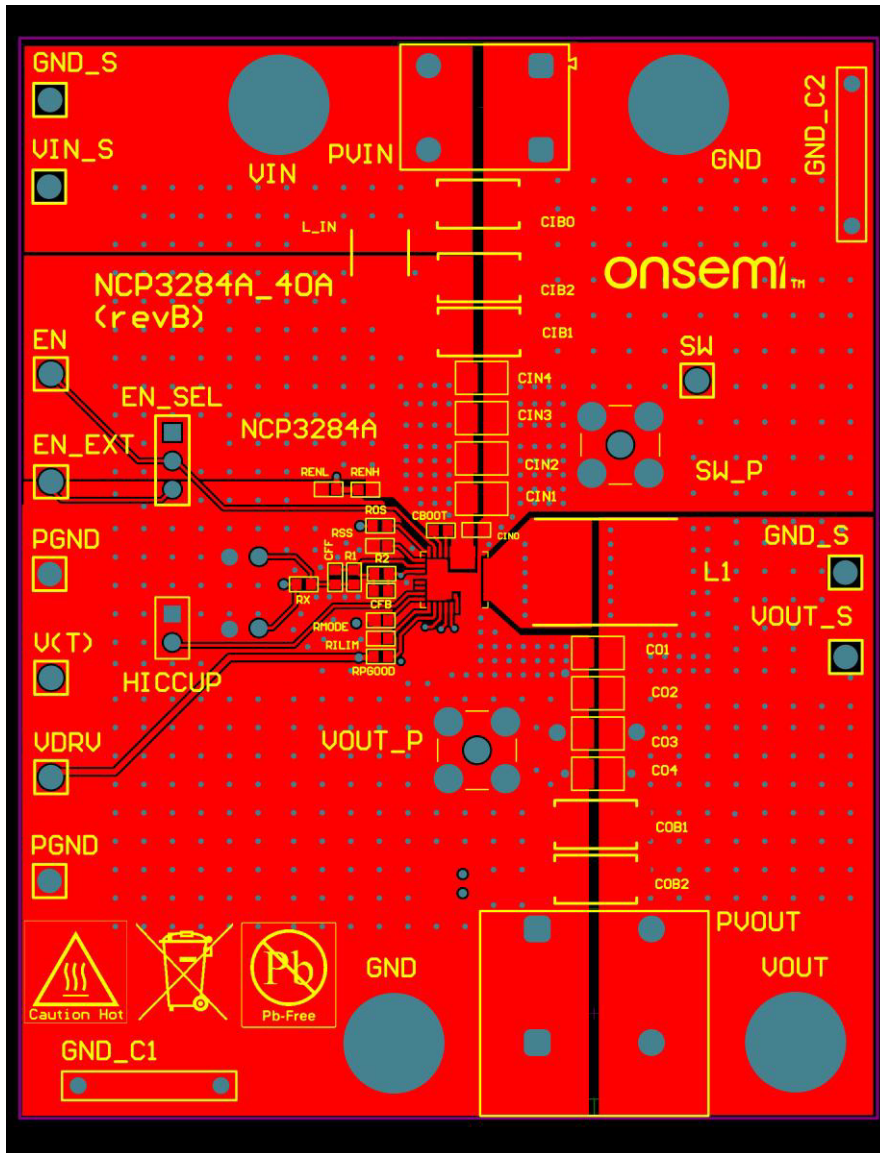


Figure 35. Top Layer (Component)

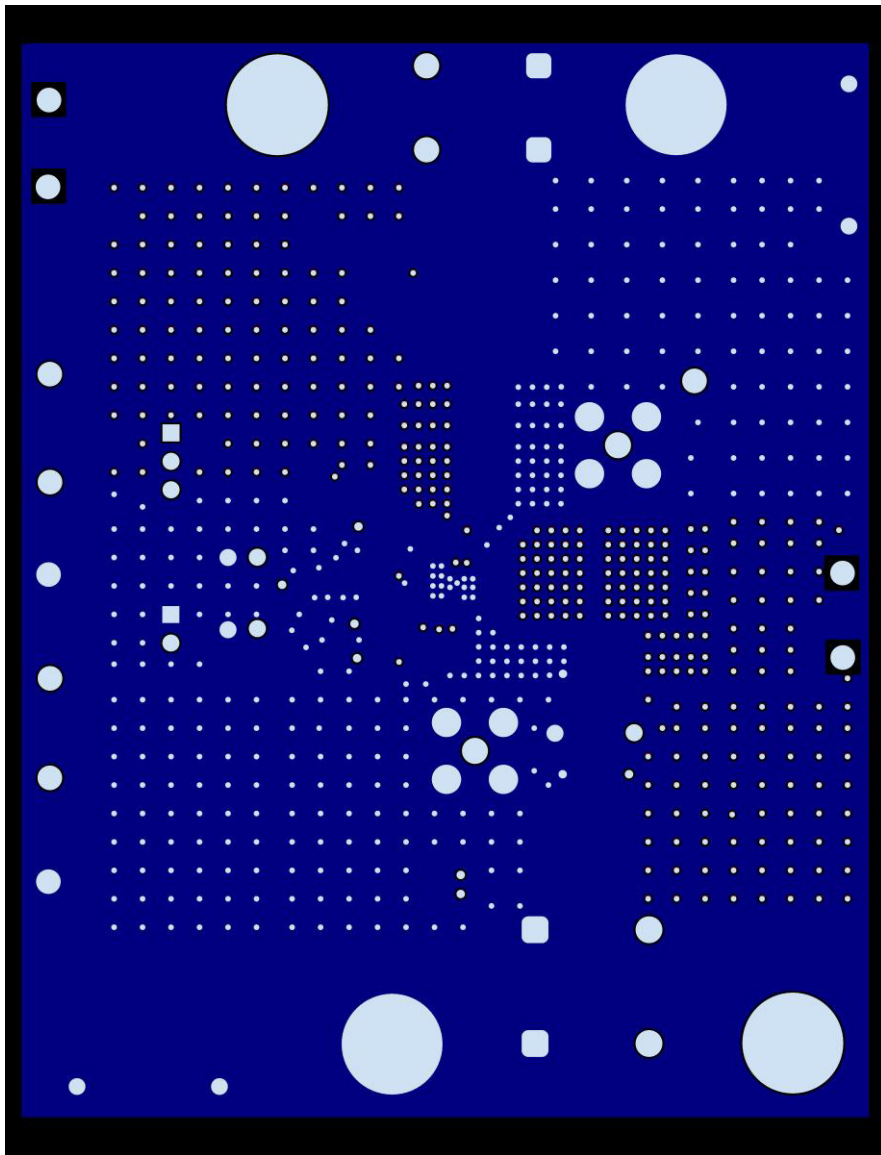


Figure 36. Mid Layer 2 (PGND Plane)

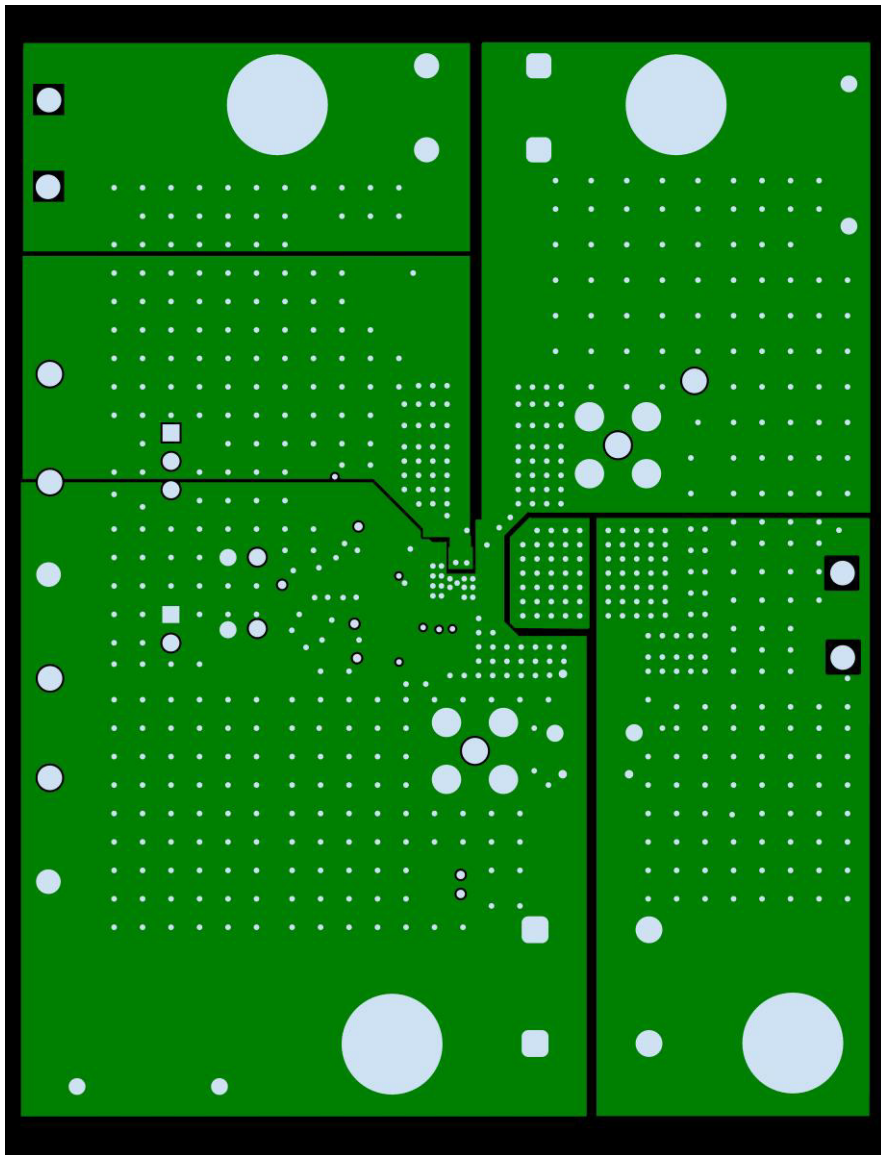


Figure 37. Mid Layer 3 (PGND, VOUT, VIN)

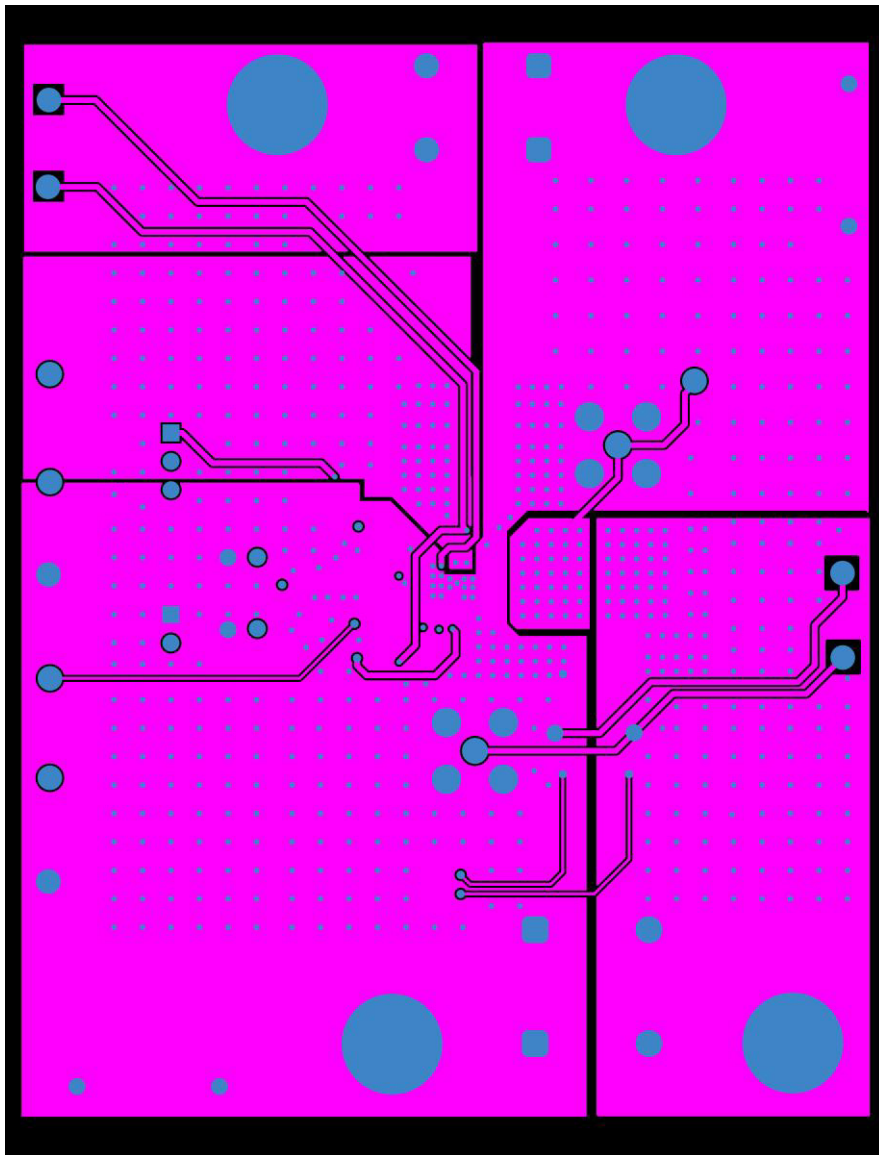


Figure 38. Mid Layer 4 (PGND, VOUT, VIN)

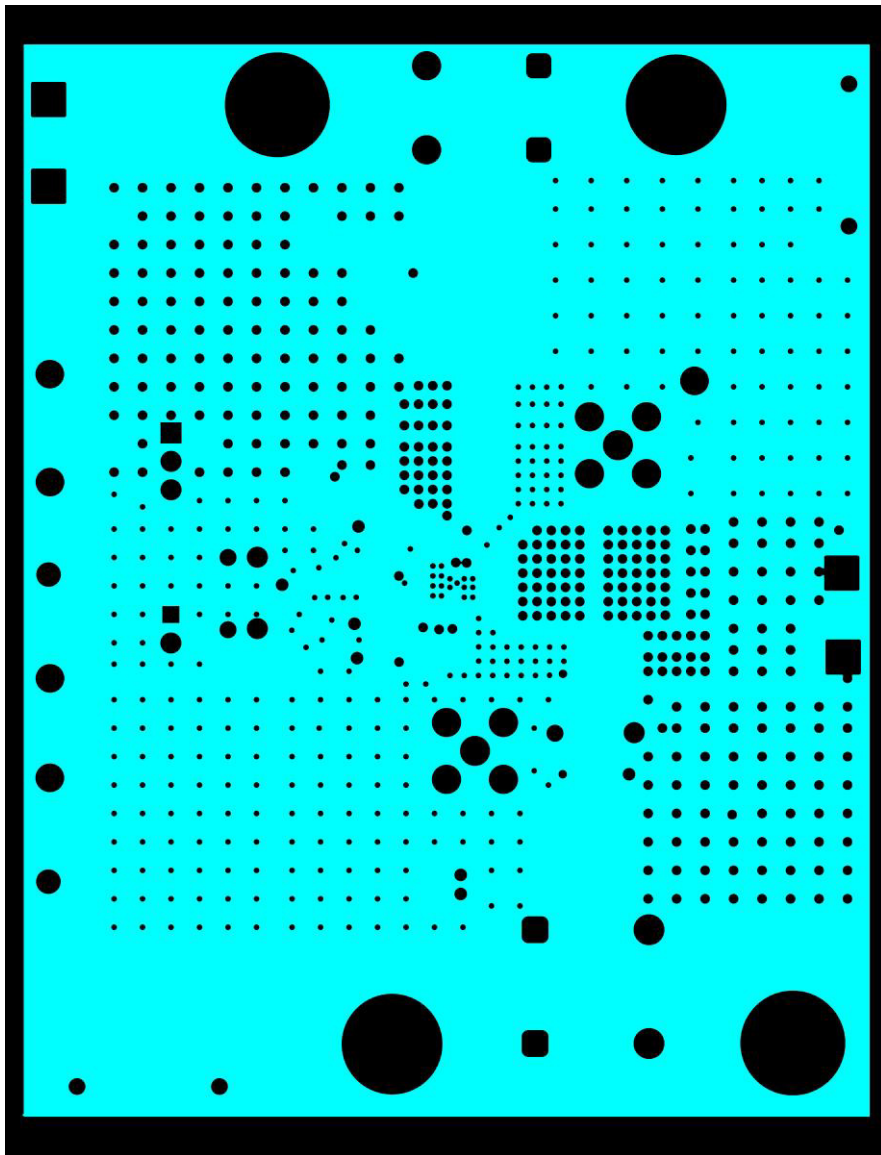


Figure 39. Mid Layer 5 (PGND)

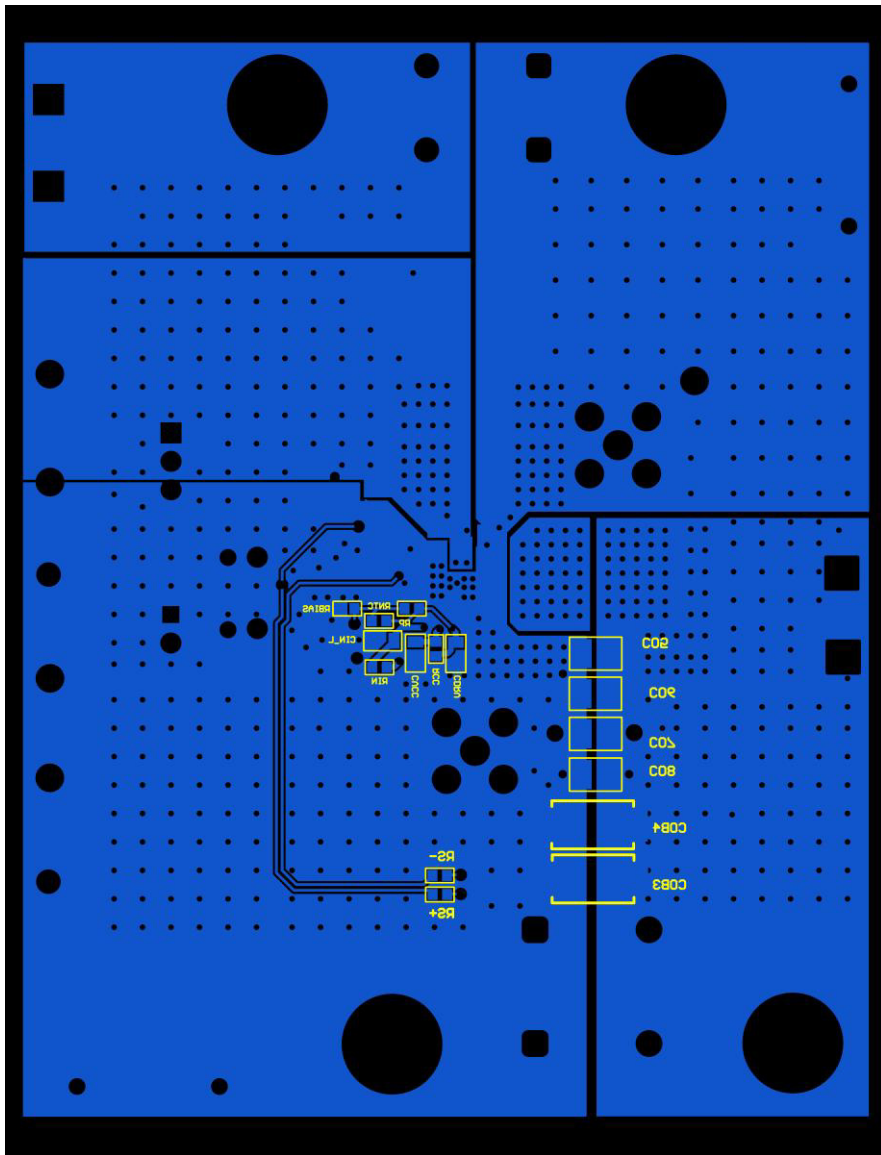


Figure 40. Bottom Layer (Component Layer)

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Table 4. BILL OF MATERIALS

Item	Description	Value	Size	Manufacturer	Rating	Part Number
PVIN	Input Power Terminal Block		10 mm pitch	Wurth Elektronik	16 A	691254810002
PVOUT	Output Power Terminal Block		10.16 mm	Wurth Elektronik	40 A	691256610002
VIN	Non-insulated Recessed Banana Jack		7.92 mm (diameter), 4.19 mm (hole)	Keystone	15 A	575-8
GND	Non-insulated Recessed Banana Jack		7.92 mm (diameter), 4.19 mm (hole)	Keystone	15 A	575-8
VOUT	Non-insulated Recessed Banana Jack		7.92 mm (diameter), 4.19 mm (hole)	Keystone	15 A	575-8
GND	Non-insulated Recessed Banana Jack		7.92 mm (diameter), 4.19 mm (hole)	Keystone	15 A	575-8
GND_C1	Ground Clip (Bus Wire)		12.7 mm pitch, 0.9 mm hole			
GND_C2	Ground Clip (Bus Wire)		12.7 mm pitch, 0.9 mm hole			
VIN_S	Test Point (Kelvin Connection for VIN+)		3.18 mm x 8.13 mm	Keystone	N/A	5011
GND_S	Test Point (Kelvin Connection for VIN-)		3.18 mm x 8.13 mm	Keystone	N/A	5010
EN	Test Point (to Device EN Pin)		3.18 mm x 8.13 mm	Keystone	N/A	5012
EN_EXT	Test Point (for External DRV)		3.18 mm x 8.13 mm	Keystone	N/A	5012
V(T)	Test Point (Mid Point of NTC Resistive Divider)		3.18 mm x 8.13 mm	Keystone	N/A	5014
VDRV	Test Point (to Device DRV Pin)		3.18 mm x 8.13 mm	Keystone	N/A	5013
PGND	Test Point (PGND Plane)		3.18 mm x 8.13 mm	Keystone	N/A	5011
VOUT_S	Test Point (Kelvin Connection to VOUT+)		3.18 mm x 8.13 mm	Keystone	N/A	5126
GND_S	Test Point (Kelvin Connection to VOUT-)		3.18 mm x 8.13 mm	Keystone	N/A	5011
SW	Test Point (to Device SW Pin)		3.18 mm x 8.13 mm	Keystone	N/A	5127
SW_P	SMA Plug (High Frequency SW Probe)		5.1 mm pitch	various	50 Ohms	
VOUT_P	SMA Plug (High Frequency VOUT Probe)		5.1 mm pitch	various	50 Ohms	
EN_SEL	3 Position 100 mil Header		100 mil pitch	various		
HICCUP	2 Position 100 mil Header (GND or Open)		100 mil pitch	various		
CIB0	Input Bulk Capacitance		2012-7343	Panasonic	25 V, 125 °C	25TDC100MD3
CIB1	Input Bulk Capacitance		2012-7343	Panasonic	25 V, 125 °C	25TDC100MD3
CIB2	Input Bulk Capacitance		2012-7343	Panasonic	25 V, 125 °C	25TDC100MD3
L_IN	Input Filter Inductor		4 mm x 4 mm x 3.1 mm	Coilcraft	20 A, 125 °C	XGL4030-131ME
L1	Power Inductor (Low Profile)	0.24 μ H	7 mm x 7 mm x 3.1 mm	Coilcraft	46 A, 125 °C	XGL7030-241ME
	Power Inductor (High Efficiency)	0.21 μ H	10.7 mm x 7.7 mm x 7.5 mm	Eaton	65 A, 125 °C	FP1108R1-R21-R
CIN0	Input Bypass (High Frequency)	1 μ F	0603	Murata	50 V, X7R	GRM188D71H105KE01#
CIN1	Input Bypass	22 μ F	1210	Murata	25 V, X7R	GCM32EC71E226KE36#
CIN2	Input Bypass	22 μ F	1210	Murata	25 V, X7R	GCM32EC71E226KE36#
CIN3	Input Bypass	22 μ F	1210	Murata	25 V, X7R	GCM32EC71E226KE36#

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Table 4. BILL OF MATERIALS (continued)

Item	Description	Value	Size	Manufacturer	Rating	Part Number
CIN4	Input Bypass	22 μ F	1210	Murata	25 V, X7R	GCM32EC71E226KE36#
CO1	Output Bypass	47 μ F	1210	Murata	10 V, X7R	GRM32ER71A476KE15#
CO2	Output Bypass	47 μ F	1210	Murata	10 V, X7R	GRM32ER71A476KE15#
CO3	Output Bypass	47 μ F	1210	Murata	10 V, X7R	GRM32ER71A476KE15#
CO4	Output Bypass	47 μ F	1210	Murata	10 V, X7R	GRM32ER71A476KE15#
CO5	Output Bypass		not populated			
CO6	Output Bypass		not populated			
CO7	Output Bypass		not populated			
CO8	Output Bypass		not populated			
COB1	Output Bulk Capacitance	330 μ F	2012-7343	Panasonic	6.3 V, 125 °C	6TCF330W9L
COB2	Output Bulk Capacitance	330 μ F	2012-7343	Panasonic	6.3 V, 125 °C	6TCF330W9L
COB3	Output Bulk Capacitance		not populated			
COB4	Output Bulk Capacitance		not populated			
CBOOT	High Side Driver (Boost) Capacitor	0.22 μ F	0603		25 V, X7R	GRM188R71H224MAC4#
RENL	Low Side Divider Resistor for VIN UVLO Circuit	27.4 k Ω	0603			
RENH	High Side Divider Resistor for VIN UVLO Circuit	95.3 k Ω	0603			
ROS	Output Voltage Sense Filter Resistor	1 k Ω	0603			
RBIAS	NTC Bias Resistor	10 k Ω	0603			
RP	NTC linearizing Resistor	40 k Ω	0603			
RNTC	NTC Thermistor	470 k Ω (@ 25 °C)	0402	TDK	β = 4306 K	NTCG044EF474FTBCX
CIN_L	Local VIN Bypass Capacitor	1 μ F	0603	Murata	50 V, X7R	GRM188D71H105KE01#
RIN	Resistor for CIN LPF	1 Ω	0603			
RILIM	Valley Current Limit Programming Resistor	33.2 k Ω	0603			
CVCC	Local VCC Bypass Capacitor	1 μ F	0603	Murata	50 V, X7R	GRM188D71H105KE01#
CDRV	5 V LDO Output Bypass Capacitor	4.7 μ F	0603	Murata	16 V, X7R	GRM188Z71C475KE21#
RCC	Low Pass Filter Resistor	2 Ω	0603			
RMODE	Frequency, DCM/CCM Setting	14 k Ω	0603			
R1	Top Side Feedback Resistive Divider	51 k Ω	0603			
		10 k Ω	0603			
R2	Bottom Side Resistive Divider	205 k Ω	0603			
		3.24 k Ω	0603			
		22 pF	0603	TDK	C0G, 50 V	CGA3E2C0G1H220J080AA
CFF	Feedforward Capacitor	33 pF	0603	TDK	C0G, 50 V	CGA3E2C0G1H330J080AA
RSS	Soft-start Programming Resistor	0 Ω	0603			
RPGOOD	PGOOD Pull-up Resistor	10 k Ω	0603			
RX	In Parallel with Signal Injection Transformer	10 Ω	0603			

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REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	6/22/2026

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